Defining the Delays of the Asynchronous Circuits

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Abstract

The purpose of the paper is that of defining the delays of a circuit as well as the properties of: determinism, order, time invariance, constancy, symmetry and the serial connection.

1 Introduction

Digital electrical engineering is a non-formalized theory and the aim of our concerns is that of trying a semi-formalization. The delay (condition) is the proposed starting point and it represents the real time model of the circuit that computes the identity function $1_{\{0;1\}}$. Logical gates and wires are modeled by a Boolean function that computes instantaneously, in real time, the output depending on the inputs and by zero, one or several delays at the output or at the inputs. The model of an asynchronous circuit consists then in the composition of the models of the logical gates and wires, meaning the serial connection of the delays and the composition of the Boolean functions.

2 Preliminaries

Definition 2.1 $\mathbf{B} = \{0;1\}$ *is endowed with the discrete topology, with the order* $0 \leq 1$ *and with the usual laws:* $^{-};\cdot;[;\oplus$.

Definition 2.2 *Let* $x : R \to B$ *and* $A \subset R$. *We define*

$$\bigwedge_{\xi\in A} x(\xi) = \begin{cases} 0; \exists \xi \in A; x(\xi) = 0 \\ 1; \text{otherwise} \end{cases} \qquad \bigwedge_{\xi\in ?} x(\xi) = 1$$

$$\bigvee_{\xi\in A} x(\xi) = \begin{cases} 1; \exists \xi \in A; x(\xi) = 1 \\ 0; \text{otherwise} \end{cases} \qquad \bigvee_{\xi\in ?} x(\xi) = 0$$

Definition 2.3 *The order and the laws of* $\mathbf{B}$ *induce an order and laws in the set of the* $R \to B$ *functions, that are noted with the same symbols.*

Definition 2.4 *Let* $x : R \to B$. *The left limit function* $x(t-0)$ *is defined by*

$$\forall t \in R; \exists \varepsilon > 0; \forall \xi \in (t-\varepsilon; t); x(\xi) = x(t-0)$$

Definition 2.5 *We suppose that* $x(t-0)$ *exists. Then the functions* $\overline{x(t-0)} \cdot x(t)$, $x(t-0) \cdot \overline{x(t)}$ *are called the left semi-derivatives of* x.

Definition 2.6 *The characteristic function* $\chi_A : R \to B$ *of the set* $A \subset R$ *is*

$$\chi_A(t) = \begin{cases} 1; t \in A \\ 0; t \notin A \end{cases}$$

Definition 2.7 *We call signal a function* x *having the property that the unbounded sequence* $0 \leq t_0 < t_1 < t_2 < \ldots$ *exists so that*

$$x(t) = x(t_0 - 1) \cdot \chi_{(-1; t_0)}(t) \oplus x(t_0) \cdot \chi_{[t_0; t_1)}(t) \oplus x(t_1) \cdot \chi_{[t_1; t_2)}(t) \oplus \ldots$$

and we note with S *the set of the signals.*

Notation 2.8 $\tau^d : R \to R$ *is the translation* $\tau^d(t) = t - d$, *where* $t; d \in R$.

Theorem 2.9 *The constant functions* $0; 1 : R \to B$ *are signals. If* $0 \leq m \leq d$ *and* $x; y \in S$, *then the functions* $x \circ \tau^d; \overline{x(t)}; x(t) \cdot y(t); x(t) \cup y(t); x(t) \oplus y(t); \bigcup_{\xi \in [t-d; t-d+m]} x(\xi); \bigcap_{\xi \in [t-d; t-d+m]} x(\xi)$ *are signals too.*

Theorem 2.10 $\forall x \in S$; *the left limit function* $x(t-0)$ *exists.*

Notation 2.11 *We note with* $P^*(S)$ *the set of the non-empty subsets of* S.

3 Stability. Rising and Falling Transmission Delays for Transitions

Definition 3.1 *Let* $u; x \in S$, *called input and respectively state (or output). The implication*

$$\forall a \in B; (\exists t_1; \forall t \geq t_1; u(t) = a) \Rightarrow (\exists t_2; \forall t \geq t_2; x(t) = a)$$

is called the stability condition (SC). We say that the couple $(u; x)$ *satisfies SC. We call also SC the function* $Sol_{SC} : S \to P^*(S)$ *defined by*

$$Sol_{SC}(u) = \{x | (u; x) \text{ satisfies SC}\}$$

Definition 3.2 *We suppose the existence of* $a \in B$ *so that* $\exists t_1; \forall t \geq t_1; u(t) = a$ *and the fact that* $(u; x)$ *satisfies SC. If* $u; x$ *are both non-constant, we note*

$$t_1^* = \min\{t_1 | \forall t \geq t_1; u(t) = a\}; \quad t_2^* = \min\{t_2 | \forall t \geq t_2; x(t) = a\}$$

The transmission delay for transitions is the number $d \geq 0$ *defined by*

$$d = \max(0; t_2^* - t_1^*)$$

If $\overline{u(t_1^* - 0)} \cdot u(t_1^*) = \overline{x(t_2^* - 0)} \cdot x(t_2^*) = 1$, *then* d *is called rising and if* $u(t_1^* - 0) \cdot \overline{u(t_1^*)} = x(t_2^* - 0) \cdot \overline{x(t_2^*)} = 1$, *then* d *is called falling. If* u, *respectively* x *is constant, then* t_1^* *respectively* t_2^* *is by definition* 0.

4 Delays

Definition 4.1 *A delay condition (DC) or shortly a delay is a function* $\mathbf{i : S \to P^*(S)}$ *with the property that* $\forall \mathbf{u; i(u) \subset Sol_{SC}(u)}$.

Remark 4.2 *The problem of the delays is that of the real time computation of the identity function* $\mathbf{1_B}$. *In practice we often work with systems of equations and inequalities in* $\mathbf{u; x}$ *that model this computation and* $\mathbf{i(u)}$ *represents for all* $\mathbf{u}$ *the set of the solutions of these systems. Definition 4.1 requests that solutions exist for any* $\mathbf{u}$ *and that the systems be stable.*

Example 4.3 *The next functions are DC's:*

- $\mathbf{i(u) = \{u\}}$ *is usually noted with* $\mathbf{I}$. *More general, the equation* $\mathbf{i(u) = \{u \circ \tau^d\}}$ *defines a DC noted with* $\mathbf{I_d; d \geq 0}$.
- $\mathbf{i(u) = \{x | \exists d \geq 0; x(t) = u(t) \cdot \chi_{[d;\,1)}(t)\}}$
- $\mathbf{i(u) = Sol_{SC}(u)}$

Theorem 4.4 *Let* $\mathbf{U \subset S}$ *and the DC's* $\mathbf{i; j}$.

a) If $\forall \mathbf{u; i(u) \wedge U \neq \emptyset}$, then the next equation defines a DC

$$\mathbf{(i \wedge U)(u) = i(u) \wedge U}$$

b) If $\mathbf{i; j}$ satisfy $\forall \mathbf{u; i(u) \wedge j(u) \neq \emptyset}$, then $\mathbf{i \wedge j}$ is a DC defined by

$$\mathbf{(i \wedge j)(u) = i(u) \wedge j(u)}$$

c) Items a), b) are generalized by taking an arbitrary function $\mathbf{' : S \to P^*(S)}$ with $\forall \mathbf{u; i(u) \wedge '(u) \neq \emptyset}$; $\mathbf{i \wedge '}$ is a DC

$$\mathbf{(i \wedge ')(u) = i(u) \wedge '(u)}$$

d) $\mathbf{i}$ and $\mathbf{j}$ define the DC $\mathbf{i \_ j}$ in the next manner:

$$\mathbf{(i \_ j)(u) = i(u) \_ j(u)}$$

5 Determinism

Definition 5.1 *The DC* $\mathbf{i}$ *is called deterministic if* $\forall \mathbf{u; i(u)}$ *has a single element and non-deterministic otherwise.*

Remark 5.2 *By interpreting* $\mathbf{i}$ *as the set of the solutions of a system, its determinism indicates the uniqueness of the solution for all* $\mathbf{u}$. *On the other hand we shall identify the deterministic DC's with the functions* $\mathbf{i : S \to S}$. *The non-deterministic delays are justified by the fact that in an electrical circuit to one input* $\mathbf{u}$ *there corespond several possible outputs* $\mathbf{x}$ *depending on the variations in ambient temperature, power supply, on the technology etc.*

Example 5.3 *In 4.3* $I; I_d$ *are deterministic and the other delays are non-deterministic. Let* $U \subset S$ *and the DC's* $i; j$ *with* i *deterministic. If* $\forall u; i(u) \wedge U \neq \emptyset$*, then* $i \wedge U (= i)$ *is deterministic and similarly for* $i \wedge j$*.*

6 The Order

Definition 6.1 *For the DC's* $i; j$ *we define*

$$i \subset j \iff \forall u; i(u) \subset j(u)$$

Remark 6.2 *The inclusion* $\subset$ *defines an order in the set of the DC's.* Sol_{SC} *is the universal element relative to this order, because any* i *satisfies* $i \subset Sol_{SC}$*. We interpret the inclusion* $i \subset j$ *by the fact that the first system contains more restrictive conditions than the second and the model in the first case is more precise than in the second one. In particular, a deterministic DC contains the maximal information and the DC* Sol_{SC} *contains the minimal information about the modeled circuit.*

Theorem 6.3 *Any DC* j *includes a deterministic DC* i*; if* $i \subset j$ *and if* j *is deterministic, then* $i = j$*.*

7 Time Invariance

Definition 7.1 *The DC* i *is called time invariant if*

$$\forall u; \forall x; \forall d \in R; (u \circ \tau^d \in S \text{ and } x \in i(u)) \Rightarrow (x \circ \tau^d \in S \text{ and } x \circ \tau^d \in i(u \circ \tau^d))$$

and if the previous property is not satisfied then i *is called time variable.*

Example 7.2 I_d *is time invariant,* $d \geq 0$*. Let the time invariant DC's* $i; j$ *with* $\forall u; i(u) \wedge j(u) \neq \emptyset$*; then* $i \wedge j$ *is time invariant. Let* k *time invariant; then* $i \_ k$ *is time invariant.* Sol_{SC} *is time variable.*

Theorem 7.3 *If* i *is a time invariant DC, then the next equivalence holds:*

$$\forall u; \forall x; \forall d \geq 0; x \in i(u) \iff x \circ \tau^d \in i(u \circ \tau^d)$$

8 Constancy

Definition 8.1 *A DC* i *is called constant if* $\exists d_r \geq 0; \exists d_f \geq 0$ *so that* $\forall u; \forall x \in i(u)$ *we have*

$$\overline{x(t-0)} \cdot x(t) \leq u(t-d_r)$$
$$x(t-0) \cdot \overline{x(t)} \leq \overline{u(t-d_f)}$$

If the previous property is not satisfied, then i *is called non-constant.*

Example 8.2 $\mathbf{I_d}$ *is constant,* $\mathbf{d \geq 0}$*. Let* $\mathbf{U \subset S}$ *and the DC's* $\mathbf{i; j}$*, the first constant. If* $\mathbf{i \wedge U}$ *and* $\mathbf{i \wedge j}$ *are defined, then they are constant. More general, any DC included in a constant DC is constant.*

Theorem 8.3 *The next functions*

$$\mathbf{x(t) = \bigcap_{\xi \in [t-d;t-d+m]} u(\xi) \quad ; \quad x(t) = \bigcup_{\xi \in [t-d;t-d+m]} u(\xi)}$$

are deterministic, time invariant, constant DC's, where $\mathbf{0 \leq m \leq d}$*.*

Remark 8.4 *Constancy means that* $\mathbf{x}$ *is allowed to switch only if* $\mathbf{u}$ *has anticipated this possibility* $\mathbf{d_r}$*, respectively* $\mathbf{d_f}$ *time units before. Its satisfaction does not imply the uniqueness of* $\mathbf{d_r; d_f}$ *and 8.3 offers such a counterexample.*

9 Rising-Falling Symmetry

Definition 9.1 *The DC* $\mathbf{i}$ *is called (rising-falling) symmetrical if*

$$\mathbf{\forall u; i(\bar{u}) = \{\bar{x} | x \in i(u)\}}$$

and respectively (rising-falling) asymmetrical otherwise.

Example 9.2 $\mathbf{I_d; d \geq 0}$ *and* $\mathbf{Sol_{SC}}$ *are symmetrical. Let the symmetrical DC's* $\mathbf{i; j}$*; if* $\mathbf{i \wedge j}$ *is defined, then it is symmetrical. The DC* $\mathbf{i \_ j}$ *is symmetrical too.*

10 The Serial Connection

Definition 10.1 *For the DC's* $\mathbf{i; j}$ *we note with* $\mathbf{k = i \circ j}$ *the function* $\mathbf{k : S \to P^*(S)}$ *defined by*

$$\mathbf{k(u) = \{y | \exists x; x \in j(u) \text{ and } y \in i(x)\}}$$

$\mathbf{k}$ *is called the serial connection of the DC's* $\mathbf{i; j}$*.*

Theorem 10.2 *The next statements are true:*

a) $\mathbf{k}$ *is a DC.*

b) *If* $\mathbf{i; j}$ *are deterministic, then* $\mathbf{k}$ *is deterministic.*

c) *If* $\mathbf{i; j}$ *are time invariant, then* $\mathbf{k}$ *is time invariant.*

d) *If* $\mathbf{i; j}$ *are symmetrical, then* $\mathbf{k}$ *is symmetrical.*

Remark 10.3 *The serial connection of the constant delays is not constant, in general. The set of the DC's is a non-commutative semi-group relative to the serial connection and* $\mathbf{I}$ *is the unit.*

Theorem 10.4 *Let the DC's* $i; j; k$. *The next implications are true:*

$$i \subset j \Rightarrow i \circ k \subset j \circ k$$
$$j \subset k \Rightarrow i \circ j \subset i \circ k$$

Theorem 10.5 *Let* $U \subset S$ *and the DC's* $i; j; k$.

a) If $\forall u; i(u) \wedge U \neq \emptyset$, then $\forall u; (i \circ j)(u) \wedge U \neq \emptyset$ and

$$(i \wedge U) \circ j = (i \circ j) \wedge U$$

If $\forall u; j(u) \wedge U \neq \emptyset$, then we have

$$i \circ (j \wedge U) \subset i \circ j$$

b) If $\forall u; i(u) \wedge j(u) \neq \emptyset$, then $\forall u; (i \circ k)(u) \wedge (j \circ k)(u) \neq \emptyset$ and

$$(i \wedge j) \circ k \subset (i \circ k) \wedge (j \circ k)$$

If $\forall u; j(u) \wedge k(u) \neq \emptyset$, then $\forall u; (i \circ j)(u) \wedge (i \circ k)(u) \neq \emptyset$ and

$$i \circ (j \wedge k) \subset (i \circ j) \wedge (i \circ k)$$

c) We have

$$(i \vee j) \circ k = (i \circ k) \vee (j \circ k)$$
$$i \circ (j \vee k) = (i \circ j) \vee (i \circ k)$$

References

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